IN THE SPECIFICATION

Please amend the paragraphs below, numbered as in the application as filed, as follows:

[0017] In accordance with this invention a method is provided for forming an RSD FET device with a recessed channel, a raised silicon S/D, and a gate electrode structure on an SOI structure, i.e. a silicon layer formed on a substrate as follows. Form a SiGe layer over the silicon layer and a RSD layer over the SiGe. Etch through the RSD layer and the SiGe to form a gate electrode space reaching down the silicon layer. Form a pair of RSD regions separated by the gate electrode space. Line the walls of the gate electrode space with an internal etch stop layer and an inner sidewall spacers. Form a gate electrode inside the inner sidewall spacers on the silicon layer. Form external sidewall spacers adjacent to the gate electrode between the RSD regions next to the inner sidewall spacers, and dope the RSD regions, whereby a recessed channel is formed in the SOI silicon layer below the SiGe layer, and with the channel located between the raised source/drain regions which are formed above the SiGe layer. Preferably, an etch stop layer is formed on the surface of the raised source drain layer before forming the gate electrode space. Preferably, the steps of forming the gate electrode space include the following steps. Form a dummy gate over the source/drain layer; form a conformal outside spacer layer over the dummy gate; form an exterior masking layer over the outside spacer layer, etching back the exterior masking layer to expose the dummy gate, and remove the dummy gate to form the gate electrode space. Preferably, the exterior masking layer is composed of silicon dioxide that covers the outside spacer layer until after filling the gate electrode space with the gate electrode and planarization thereof. Preferably, the exterior masking layer is composed of silicon germanium (SiGe) which covers the outside spacer layer until after filling the gate electrode space with the gate electrode and planarization thereof and after recessing the outside spacer layer down to the etch stop layer. Preferably, the insulator forming the substrate comprises silicon oxide. Preferably, an etch stop layer is formed on the surface of the raised source drain layer before forming the gate electrode space, and the exterior masking layer is composed of silicon germanium (SiGe) which covers the outside spacer layer until after filling the gate electrode space with the gate electrode and planarization thereof and after recessing the outside spacer layer down to the etch stop layer. Preferably, an etch stop layer is formed on the surface of the raised source drain layer before forming the gate electrode space; the exterior masking layer is composed of silicon germanium (SiGe) which covers the outside spacer layer until after filling the gate electrode space with the gate electrode and planarization thereof. After recessing the outside spacer layer down to the etch stop layer, perform a raised source extension region and a raised drain extension region implant and then form an exterior spacer aside from the gate electrode.

[0018] In accordance with another aspect of this invention, a method is provided for forming an FET device with a raised silicon source/drain and a gate electrode structure on an SOI structure comprising an SOI silicon layer formed on a substrate. The ~~wherein the~~ substrate comprises an insulator. A , ~~whereby a~~ recessed channel is formed in the SOI silicon layer below the SiGe layer with the recessed channel located between the raised source/drain regions which are formed above the SiGe layer. The steps of the method are as follows. Form a SiGe layer over the silicon layer. Form a raised source/drain layer over the SiGe layer. Form an etch stop layer over the raised source/drain layer. Form a dummy gate over the source/drain layer. Form a conformal outside spacer layer over the dummy gate. Form an exterior masking layer over the outside spacer layer. Etch back the exterior masking layer to expose the dummy gate. Remove the dummy gate to form the gate electrode space etching through the raised source/drain layer and the SiGe layer to form a gate electrode space with walls reaching down through the raised source/drain layer and the SiGe layer to the surface of the silicon layer thereby forming a pair of raised source/drain regions separated by the gate electrode space in the source/drain layer. Line the walls of the gate electrode space with an internal etch stop layer and an inner sidewall spacers. Form a gate electrode inside the inner sidewall spacers on a cleaned surface of the silicon layer. Form external sidewall spacers adjacent to the inner sidewall spacers. Dope the source/drain regions.

[0022] ~~In accordance with another aspect of this invention, an FET device with a raised silicon source/drain and a gate electrode structure is formed on an SOI structure comprising an SOI silicon layer formed on a substrate wherein the substrate comprises an insulator. A SiGe layer is formed over the silicon layer. A raised source/drain layer is formed over the SiGe layer. A gate electrode space with walls reaching down through the raised source/drain layer and the SiGe layer to the surface of the silicon layer forms a pair of raised source/drain regions separated by the gate electrode space in the source/drain layer. The walls of the gate electrode space are lined with an internal etch stop layer and inner sidewall spacers. A gate electrode is formed inside the inner sidewall spacers on a cleaned surface of the silicon layer. A gate electrode is formed within the space inside the inner sidewall spacers. External sidewall spacers are formed adjacent to the inner sidewall spacers. Doped the source/drain regions are formed in the raised source/drain layer. There is a recessed channel in the SOI silicon layer between the raised source/drain regions above the SiGe layer.~~

[0035] FIG. 1B shows a device [[10"]] 10' which is a second embodiment of the present invention, which is a modification of FIG. 1A. Device 10' [[10"]] is formed on an SOI (Silicon on Oxide) substrate composed of a thick BOX layer 12 upon which a thin silicon layer 14 has been formed. The silicon layer 14 has been coated (preferably by epitaxial growth of SiGe from Si) with a thin SiGe film 16 and [[the]] a set of RSD' (RS'/RD') ~~(RS"/RD")~~ regions 18' [[18"]] have been formed over the SiGe film 16 (preferably by epitaxial growth of Si from SiGe).

[0036] However in the case of FIG. 1B, the RSD' regions 18' [[18"]] are separated from the thin silicon oxide internal etch stopping film 28 by the external sidewall spacers 36' [[36"]] composed of a dielectric material preferably selected from the group consisting of silicon nitride, silicon oxide and oxynitride. The external sidewall spacers [[36"]] 36', which cover the RSD' regions 18'D, reach down into contact with the top surface of the SiGe layer 16 between the internal etch stopping film 28 on the inside and the RSD' regions 18' [[18]] on the outside.

[0037] In FIG. 1B, as in FIG. 1A, in the center of the device 10' [[10"]] an elevated trench (above the silicon layer 14 of the SOI substrate) has been formed down to the surface of the silicon layer 14. The trench has been lined with a thin dielectric layer comprising gate dielectric layer GD at the base thereof plus thin silicon oxide internal etch stopping film 28 lining the sidewalls of the trench above the gate dielectric layer GD. Again tapered silicon nitride inner sidewall spacers 30 have been formed on the sidewalls of the thin silicon oxide layer 28 leaving a central opening in the trench ~~opening~~ reaching down to the top surface of the gate dielectric layer GD. The trench has been filled with a gate conductor 32 which will serve as the gate electrode of the MOS FET device which is isolated from the silicon layer 14 by the gate dielectric layer GD and which is protected by the tapered dielectric inner sidewall spacers 30 and the internal etch stopping film 28.

[0038] In FIG. 1B, the structure of FIG. 1A has been modified so that above the RSD' regions 18' [[18]] adjacent to the gate conductor 32, on the outside of the internal etch stopping film 28, the external sidewall spacers 36' [[36"]] are formed outside of the internal etch stopping film 28 reaching down below the raised silicon layer 18' to the top of the SiGe film 16. The external sidewall spacers 36' [[36"]] are composed of a material preferably selected from the group consisting of silicon oxide, silicon nitride and oxynitride. The thin dielectric etch stop layer 20 has been omitted from the final product in the embodiment in FIG. 1B.

[0039] As in FIG. 1A, the SiGe film 16 and the top Si layer 18' [[18"]] are provided as etch stoppers to obtain good control of the channel thickness, which is important for the control of Vt, mobility, and the Short Channel Effect (SCE) of a device such as the UT-SOI device 10 of FIG. 1A.

[0041] FIG. 1C shows a device 10", that is a third embodiment of the present invention which is a modification of the device 10' of FIG. 1B. As in FIG. 1B, the device 10" of FIG. 1C is formed on an SOI (Silicon on Oxide) substrate composed of a thick BOX layer 12 upon which a thin silicon layer 14 has been formed, and the silicon layer 14 has been coated with a thin SiGe film 16" and the set of RSD" regions RS"/RD" have been formed over the SiGe film 16".

[0042] But in FIG. 1C, ~~the this case~~ both the thin SiGe film 16" and the RSD" regions RS"/RD" 18 are separated from the thin silicon oxide internal etch stopping film 28 by the external sidewall spacers 36" composed of silicon nitride or silicon oxide layer, which cover the RSD" regions RS"/RD" and reach down into contact with the top surface of the Si layer 14 (below the SiGe film 16") between the internal etch stopping film 28 on the inside and the RSD" regions RS"/RD" and the SiGe film 16" on the outside.

[0043] As in FIGS. 1A and 1B, in the center of the device 10" of FIG. 1C, an elevated opening (such as the opening 22L in FIG. 2H [[2G]]) above the silicon layer 14 of the SOI substrate) has been formed down to the surface of the silicon layer 14. The trench has been lined with a thin dielectric layer comprising a gate dielectric layer GD at the base thereof, plus a thin silicon oxide internal etch stopping film 28, and inner sidewall spacer layer 30 (preferably composed of silicon nitride) lining the sidewalls of the trench above the gate dielectric layer GD, providing a narrower opening, [[(]] such as narrowed opening 22M in FIG. [[2H).]] 2I. Again, tapered silicon nitride inner sidewall spacers 30 have been formed on the sidewalls of the thin internal etch stopping film 28, [[(]] e.g. silicon oxide, [[)]] leaving a central opening, [[(]] such as gate electrode opening 22N in FIG. 2J, [[2I)]] down to the surface of the gate dielectric layer GD. The trench has been filled with a gate conductor 32 which will serve as the gate electrode of the MOS FET device which is isolated from the silicon layer 14 by the gate dielectric layer GD; and which is protected by the tapered dielectric inner sidewall spacers 30 and the internal etch stopping film 28.

[0050] Initially, as shown in FIG. 2A a thin, blanket, monocrystalline SiGe layer 16 has been formed over the monocrystalline silicon layer 14 of device 50. The SiGe layer 16 comprises a monocrystalline layer formed by epitaxial growth of silicon germanium (SiGe) alloy (Si with about 10 to 20% of Ge) over the silicon layer 14.

[0052] FIG. 2A also shows the device 50 after growth of a thicker, blanket, undoped, monocrystalline, raised silicon (Si) layer 18 by epitaxial deposition [[on]] onto the surface of the thin SiGe layer 16. The raised Si layer 18 is deposited to be formed into the raised source/drain (RSD) regions 18 later in the process. The raised Si layer 18 is thicker than the SiGe layer 16.

[0054] FIG. 2B shows the device 50 of FIG. 2A after deposition of a blanket thin first etch stop layer 20 composed of a material preferably selected from the group consisting of silicon oxide, silicon nitride and oxynitride to be followed by deposition of a blanket dummy (sacrificial) gate layer 22 (shown in FIG. 2C) composed of a thick blanket layer of a material such as polysilicon.

[0058] In an alternative embodiment (not shown), the extensions and source drain implants and silicide may be formed in the next step. In this case the use of a high k dielectric and metal gate may be used after removal of the dummy gate 22D, which is shown in FIG. 2D and which is formed in step 5.

[0070] FIG. 2H shows the device 50 of FIG. 2G after removal of the dummy gate 22D (preferably by etching it away) to form a shallow portion of the opening for trench 22L. Then the opening which is being formed as trench 22L is deepened by the following step of anisotropically etching away the exposed portions of first etch stop layer 20, as well as the RSD layer 18 and the SiGe film 16 down to the surface of the thin silicon film 14. The etching yields a high quality planar Si surface. This method can be also used to produce stress in the channel due to relaxation of stress in the strained SiGe film 16, and to produce compressive stress in the channel of the device. Compressive stress can enhance PMOS FET performance.

[0072] FIG. 2I shows the device 50 of FIG. 2H after an internal etch stopping film 28B is deposited conformally, which is preferably composed of thin silicon oxide (SiO_2), to serve as an etch stopper for the internal spacer film [[30]] 30B. Next, as also shown by FIG. 2I, [[an]] the internal spacer film 30B (preferably composed of silicon nitride) is deposited conformally over the internal etch stop film 28B, narrowing the opening forming trench 22L [[down]] leaving a narrower and shallower opening 22M.

[0121] FIG. 3N shows the device [[50]] 60 of FIG. 3M after stripping away the exterior masking layer 126, thereby exposing the sacrificial outside spacer layer 124. The method of removing the SiGe layer 126 is a non-hydrogen containing etch gas mixture. The etch may be a plasma etch and continues through the SiGe selective to Si. In this case the poly-Si gate 32 will not be etched. (Here if one were to use silicon oxide as the sacrificial outside spacer layer 124, instead of SiGe in step 6 of the fifth embodiment, the etching of the silicon oxide of the sacrificial outside spacer layer 124 the top of silicon nitride exterior masking layer 126, may attack the internal etch stop film 28 (silicon oxide (SiO_2)) on the silicon nitride inner spacer sidewall 30.

[0125] FIG. 3O also shows the device 60 after, a different selective, anisotropic, RIE step is performed, also using the sacrificial outside spacer layer 124 as a mask, to remove the exposed portion of the raised silicon layer 18 stopping on the thin SiGe layer 16 and leaving a recess 140 below where recess 130 had been in FIG. 3N. At the same time, the height of the gate 32 is lowered to an equal degree to the raised silicon layer 18 forming a shortened gate 32' [[32'']], leaving the inner spacers 30 and the internal etch stop film 28 extending thereabove. In addition, the regions RE of the SiGe layer 16 are exposed between the raised silicon structures 18 and the shortened gate 32' [[32'']].

[0129] FIG. 3P shows the device [[50]] 60 of FIG. 3O with the shortened gate electrode 32' [[155]] shown, in an intermediate stage of completion, after stripping the remainder of the first etch stop layer 20 (which had been protected by the sacrificial outside spacer layer 124) by an anisotropic RIE etching step. This leaves the surface of the raised silicon layer 18 exposed. If the first etch stop layer 20 is composed of silicon oxide (SiO_2), an anisotropic RIE step is performed to strip the etch stop layer 20. This etching step may also etch away some of the exposed portions of the internal etch stop film 28, which is exposed by the formation of the recess 129 in FIG. 3M, recess 130 in FIG. 3N and recess 140 in FIG. 3O.

[0131] FIG. 3Q also shows the device 60 of FIG. 3P after performing an etch to lower the inner sidewall spacers 30 to the level of the shortened gate electrode 32' [[32"]], which was lowered in step 17.

[0135] FIG. 3R shows the device 60 of FIG. 3Q after removal of the remainder of the internal etch stop film 28 leaving the inner sidewall spacers 30 exposed adjacent to the shortened gate electrode 32' [[165]]. If the internal etch stop film 28 is composed of silicon oxide (SiO_2) the preferred method of stripping thereof is to perform a wet etch with a hydrogen fluoride bath.

[0140] Step 24: Form External Sidewall Spacer

FIG. 3U shows the device 60 of FIG. 3T after formation of external sidewall spacers 36 on the outer sidewalls of the inner sidewall spacers 30. The external sidewall spacers 36 are preferably composed of silicon nitride to control S/D diffusion.

[0144] FIG. 3W shows the device 60 of FIG. 3V after a conventional S/D anneal of the RSD regions 18. FIG. 3W shows the device 60 of FIG. 3V after a conventional S/D anneal (preferably RTA, spike or non-melt laser anneal. After this step, one can follow conventional processing to finish the processing of the device (silicidation and making contacts, etc., as will be well understood by those skilled in the art. The recessed channel is located below the gate 32' [[32"]] in FIG. 3W in the SOI silicon 14 between the spacers 36 [[34]].